IN THE CLAIMS:

Please amend the claims as set forth below:

1. (Currently Amended) An apparatus comprising:

a first storage location configured to store a segment selector identifying a segment descriptor including a first operating mode ~~indication and~~ indication, a second operating mode indication, and one or more indications that identify a segment described by said segment descriptor as a code segment;

a second storage location configured to store an enable indication, wherein said enable indication, said first operating mode indication, and said second operating mode indication are indicative of a default address size ~~an operating mode~~; and

a processor configured to process an instruction ~~according to said operating mode~~ using said default address size.

2. (Currently Amended) The apparatus as recited in claim 1 wherein said default address size ~~operating mode~~ is a first address size ~~operating mode~~ if said enable indication is in an enabled state and said first operating mode indication is in a first state, and wherein said ~~operating mode~~ default address size is a second address size ~~operating mode~~ if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state.

3. (Currently Amended) The apparatus as recited in claim 2 wherein said second ~~operating mode~~ address size is one of a plurality of address sizes ~~operating modes~~ available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of address sizes ~~operating modes~~ is selected in response to a state of said second operating mode

indication.

4. (Currently Amended) The apparatus as recited in claim 3 wherein one of said plurality of address sizes ~~operating modes~~ is a 32 bit address size ~~operating mode~~.

5. (Currently Amended) The apparatus as recited in claim 3 wherein one of said plurality of address sizes ~~operating modes~~ is a 16 bit address size ~~operating mode~~.

6. (Currently Amended) The apparatus as recited in claim 2 wherein said first ~~operating mode includes a default~~ address size ~~which~~ is greater than 32 bits.

7. (Currently Amended) The apparatus as recited in claim 6 wherein, if said enable indication is in said enabled state and said first operating mode indication is in said first state, said processor is configured to process said instruction using ~~said first operating mode further includes~~ a default operand size of 32 bits.

8. (Original) The apparatus as recited in claim 2 wherein said segment descriptor is one of a plurality of segment descriptors stored in a descriptor table including a plurality of entries, and wherein at least one of said plurality of segment descriptors occupies two of said plurality of entries.

9. (Original) The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is a call gate descriptor.

10. (Original) The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is an interrupt gate descriptor.

11. (Original) The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is a trap gate descriptor.

12. (Original) The apparatus as recited in claim 8 wherein said one of said plurality of

segment descriptors is a task state segment descriptor.

13. (Original) The apparatus as recited in claim 8 wherein said one of said plurality of segment descriptors is a local descriptor table descriptor.

14. (Original) The apparatus as recited in claim 1 wherein said first storage location is a memory location.

15. (Original) The apparatus as recited in claim 1 wherein said first storage location is a general purpose register within said processor.

16. (Original) The apparatus as recited in claim 1 wherein said first storage location is a special purpose register within said processor.

17. (Original) The apparatus as recited in claim 1 wherein said second storage location is a memory location.

18. (Original) The apparatus as recited in claim 1 wherein said second storage location is a general purpose register within said processor.

19. (Original) The apparatus as recited in claim 1 wherein said second storage location is a special purpose register within said processor.

20. (Original) The apparatus as recited in claim 1 wherein said processor is configured to process said instruction by executing interpreter software which emulates said instruction.

21. (Original) The apparatus as recited in claim 1 wherein said processor is configured to process said instruction by executing translation software to translate said instruction into one or more native instructions to be executed by said processor.

22. (Currently Amended) The apparatus as recited in claim 1 wherein, if said enable indication is in a disabled state, said first operating mode indication is undefined and said second operating mode indication is indicative of said default address size ~~operating mode~~.

23. (Currently Amended) A method comprising:

determining a default address size ~~an operating mode~~ in response to an enable indication in a first storage location, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor, wherein said segment descriptor further includes one or more indications that identify a segment described by said segment descriptor as a code segment;

~~fetching operands and~~ generating addresses in response to said default address size ~~operating mode~~.

24. (Currently Amended) The method as recited in claim 23 wherein said determining comprises ~~determining~~ selecting a first address size as said default address size ~~operating mode~~ responsive to said enable indication being in an enabled state and said first operating mode indication being in a first state, and wherein said first ~~operating mode includes a default~~ address size is greater than 32 bits.

25. (Currently Amended) The method as recited in claim 24 ~~wherein said first operating mode includes~~ further comprising determining a default operand size of 32 bits in response to said enable indication in said first storage location, said first operating mode indication in said segment descriptor, and said second operating mode indication in said segment descriptor.

26. (Original) The method as recited in claim 23 wherein said segment descriptor is one of a plurality of segment descriptors stored in a descriptor table having a plurality of

entries, the method further comprising reading a second segment descriptor of said plurality of segment descriptors from said segment descriptor table, wherein said second segment descriptor occupies up to two entries of said plurality of entries depending upon a type of said second segment descriptor.

27. (Original) The method as recited in claim 26 wherein said second segment descriptor is a call gate descriptor.

28. (Original) The method as recited in claim 26 wherein said second segment descriptor is an interrupt gate descriptor.

29. (Original) The method as recited in claim 26 wherein said second segment descriptor is a trap gate descriptor.

30. (Original) The method as recited in claim 26 wherein said second segment descriptor is a task state segment descriptor.

31. (Original) The method as recited in claim 26 wherein said second segment descriptor is a local descriptor table descriptor.

32. (Currently Amended) The method as recited in claim 24 wherein said determining further comprises ~~determining~~ selecting a second address size as said default address size ~~operating mode~~ responsive to said enable indication being in an enabled state, said first operating mode indication being in a second state, and said second operating mode indication being in said first state, and wherein said second address size is ~~first operating mode includes a default address size of~~ 32 bits.

33. (Currently Amended) The method as recited in claim 24 wherein said determining further comprises ~~determining~~ selecting one of a plurality of address sizes as said default address size ~~operating modes~~ if said enable indication is in said enabled state and said first operating mode indication is in a second state, and wherein said one of said plurality

of ~~operating modes~~ address sizes is selected in response to a state of said second operating mode indication.

34. (New) A computer readable medium storing a plurality of native instructions executable directly on a processor, wherein the plurality of native instructions comprise native instructions which, when executed, perform one or more operations defined for a non-native instruction using a default address size, the default address size determined in response to an enable indication in a first storage location, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor, wherein said segment descriptor further includes one or more indications that identify a segment described by said segment descriptor as a code segment.

35. (New) The computer readable medium as recited in claim 34 wherein the native instructions emulate the non-native instruction.

36. (New) The computer readable medium as recited in claim 34 wherein the native instructions are generated by compiling the non-native instruction.

37. (New) The computer readable medium as recited in claim 34 wherein said default address size is a first address size if said enable indication is in an enabled state and said first operating mode indication is in a first state, and wherein said default address size is a second address size if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state.

38. (New) The computer readable medium as recited in claim 37 wherein said second address size is one of a plurality of address sizes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of address sizes is selected in response to a state of said second operating mode indication.

39. (New) The computer readable medium as recited in claim 38 wherein one of said plurality of address sizes is a 32 bit address size.

40. (New) The computer readable medium as recited in claim 38 wherein one of said plurality of address sizes is a 16 bit address size.

41. (New) The computer readable medium as recited in claim 37 wherein said first address size is greater than 32 bits.

42. (New) The computer readable medium as recited in claim 41 wherein, if said enable indication is in said enabled state and said first operating mode indication is in said first state, said native instructions use a default operand size of 32 bits.

43. (New) The computer readable medium as recited in claim 37 wherein said segment descriptor is one of a plurality of segment descriptors stored in a descriptor table including a plurality of entries, and wherein at least one of said plurality of segment descriptors occupies two of said plurality of entries.

44. (New) The computer readable medium as recited in claim 43 wherein said one of said plurality of segment descriptors is a call gate descriptor.

45. (New) The computer readable medium as recited in claim 43 wherein said one of said plurality of segment descriptors is an interrupt gate descriptor.

46. (New) The computer readable medium as recited in claim 43 wherein said one of said plurality of segment descriptors is a trap gate descriptor.

47. (New) The computer readable medium as recited in claim 43 wherein said one of said plurality of segment descriptors is a task state segment descriptor.

48. (New) The computer readable medium as recited in claim 43 wherein said one of said plurality of segment descriptors is a local descriptor table descriptor.

49. (New) The computer readable medium as recited in claim 34 wherein said first storage location is a memory location.

50. (New) The computer readable medium as recited in claim 34 wherein said first storage location is a general purpose register within said processor.

51. (New) The computer readable medium as recited in claim 34 wherein said first storage location is a special purpose register within said processor.